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A Generalized Switched Inductor Cell Modular Multilevel Inverter

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***Abstract*—An interesting feature of Z-source inverter is to provide buck-boost ability in a single stage. However, this concept is most popular in conventional inverters. In a few multilevel inverters, Z-source is utilized to have higher gain along with retaining the advantages of multilevel inverter such as better EMI compatibility, low harmonic distortion, etc. However, the potential of the Z-source concept is not fully exploited in multilevel inverters. To widen the feasibility of Z-source concept in the multilevel inverter, a modular multilevel inverter is considered. In this paper, a generalized switched inductor cell is selected as a Z-source network for integration, however, other Z-source networks such as quasi boost network, quasi switched boost network, two winding coupled inductor network, three winding coupled inductor network, etc. may be used in place of switched inductor cell. The quantitative and qualitative analysis is done for the proposed converter in both the continuous current mode and discontinuous current mode. The analysis shows that a higher voltage gain can be achieved in the discontinuous current mode as compared to the continuous current mode. To control the proposed converter, two new modulation techniques are proposed i.e. full shoot through and upper shoot through/lower shoot through. Finally, the proposed converter is validated experimentally in both the modes and for different modulation techniques.**

***Index Terms*—Continuous Current Mode, Discontinuous Current Mode, Multilevel Inverter, Z-Source Inverter**

I. Introduction

In recent years, the interest in renewable energy is increased sharply due to high power demand. Renewable energy provides a sustainable solution with the eco-friendly environmental condition. Various categories of renewable energy resources are available such as wind energy, geothermal energy, solar energy, etc. Among them, solar energy is readily available which is extracted using PV panels [1]. In the last few years, solar power plants are established for different capacity (ranging from KW to MW) in large number. The PV panels produce DC voltage which is quite low to be considered as sufficient for real-world applications. Besides this, most of the consumer devices are of AC type, therefore, a DC to AC converter is required with PV. Though traditional voltage source inverter (VSI) can provide AC voltage, it has the following limitation: 1) VSI is a buck inverter. 2) produces higher total harmonic distortion (THD), 3) sensitive to electromagnetic interference(EMI), 4) high rate of change of voltage($\frac{dv}{dt}$), 5) higher voltage stress across inverter switches.

Except for boosting the voltage level, multilevel inverter (MLI) is a potential candidate to improve the limitation of VSI [2]. The core idea behind the introduction of MLI is to reduce THD, low EMI issues, low rate of change of voltage($\frac{dv}{dt}$), smaller filter requirement and reduced voltage stress across the switch [3]. Consequently, MLI offers higher efficiency and better reliability but at the cost of higher number of switches. Mainly, MLI's are categorized into three types: Cascaded multilevel inverter(CMLI) [4], Flying capacitor(FC) [5] and Neutral point clamped inverter (NPC) [6]. FC and NPC MLI both utilize the capacitor and diode arrangement to clamp the undesired signals. Therefore, the number of passive elements and diode get increased. In particular, the presence of the capacitor makes the circuit cumbersome. Moreover, to avoid the circulating current issues capacitor must be balanced which is difficult in a practical scenario. To solve these issues, CMLI is introduced. The CMLI configuration uses H-bridge structures to produce different voltage level. The distinct features of CMLI include balanced loading and constant switching frequency [7]. Nevertheless, the increased levels come with increased H-bridge structure which increases the size and cost of the inverter. Moreover, CMLI requires isolated DC source which may create unbalanced situation provided that voltage is not distributed equally. Besides certain advantage and disadvantage of FC, NPC, and CMLI, the main issue is, these topologies intrinsically has voltage buck capability. Although this limitation can be avoided by having multiple voltage source topologies but this not feasible solution from the cost and control point of view.

It is obvious that boosting the voltage in the multilevel inverter is a challenging issue for the renewable application. To mitigate this issue, the Z-source inverter concept may be utilized for MLI. Z-source inverter provides the buck-boost feature in a single stage, better EMI compatibility and shoot through protection [8]–[10]. Loh et al explored the uses of Z-source concept in the conventional NPC which has two voltage source [11], [12]. Two conventional Z-source networks are selected for integration. However, the number of passive elements are higher. To reduce the number of elements, a single Z-source network is utilized along with single split DC source [13]. But the stress across the capacitor is double as compared to conventional NPC which increases the size. Therefore, there is a trade-off between the selection of a Z-source network. To improve the gain of the Z-source based NPC, Trans Z-source and Γ Z-source is also reported [14]. However, the input current for the reported networks is discontinuous which increases the current stress on the DC source. The different quasi Z-source networks are reported with MLI to overcome the issue of discontinuous current [15]–[17]. To

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reduce the stress across the capacitor, Yu et al. proposed a new quasi Z-source based MLI [18]. The quasi Z-source network is also reported for CMLI's [19], [20]. However, the presence of multiple DC source requires multiple quasi Z-source network, consequently, the number of passive elements increases which increases the size and cost of the system. Therefore, the current challenge is to reduce the number of active or passive or both types of elements to improve the power density and efficiency for the Z-source based MLI.

To achieve the objective of reducing the number of active or passive or both types of elements to improve the power density and efficiency, in this paper, the authors propose a better solution in the category of Z-source based MLI. The present paper utilizes a modular multilevel inverter(MMLI) which has a lower number of passive and active element counts and consequently has better effciency [21]. To bring the Z-source feature in the MMLI, a generalized switched inductor approach is considered. However, any reported Z-source network such as quasi Z-source [22]–[25], switched boost [26], [27], switched Z-source [28], coupled inductor network [29] etc. may be utilized in the proposed configuration. The proposed configuration is named as switched inductor modular multilevel inverter(SL-MMLI) [30]. The SL-MMLI is analyzed for n-the number of switched inductor cells, analytically in both continuous current mode(CCM) and discontinuous current mode(DCM). It is proved that SL-MMLI operating in DCM has higher gain as compared to CCM. Moreover, two modulation techniques are proposed to control the proposed inverter. Finally, an experimental set up is designed and tested for one switched inductor cell and results corresponding to the different operating condition are reported.

Rest of the paper is organized as follow: Section II discusses the brief about the Z-source inverter and motivation behind the proposed study followed by the operating principle of the proposed inverter in section III. The steady-state analysis and control of the proposed inverter are elaborated in section IV and section V, respectively. The validation of the proposed inverter is illustrated in section VI. At last, the conclusion is presented in section VII.

II. Revisit of Z-Source Converter and Motivation

Z-source inverters are playing an important role in boosting the voltage level with better EMI compatibility and single-stage conversion [31]. Therefore, Z-source inverters are a highly reliable system. The primitive structure of Z-source inverter is shown in Fig-1, which consists of a symmetrical arrangement of L and C elements along with diode. The most important feature of the Z-source inverter is, it increases the utilization factor by use of zero state present in the VSI as the shoot-through state. The shoot-through state is optimized in such a fashion that the zero state never comes into the picture. The shoot-through state can be applied by 7 different ways which are dependent on the inverter legs. In conventional VSI, eight states are present, hence, Z-source inverter consists of 15 states. However, these states can be reduced to 13 states if the shoot-through state is optimized such that the period for zero state becomes zero. During shoot-through states, inductor present in the inverter charges while it delivers the power to the load during active states. Based on this, several Z-source topologies had been reported. However, most of them are on two levels. It has been also applied in NPC and CMLI but the number of active or passive elements is a major concern. This motivated us to implement the Z-source concept in a better modular multilevel inverter.

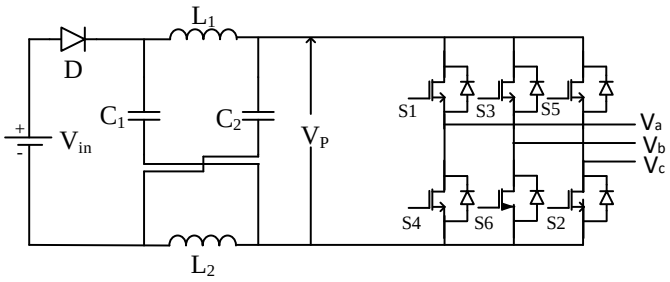

Fig. 1: Conventional Z-source Inverter

III. Topology and operation of Proposed Converter

A. Topology introduction

The core idea behind the introduction of modular multilevel inverters(MMLI) was to improve the THD at the load end. Various MMLI had been reported to date. These topologies are different in two aspects amongst Number of switches(Active or passive) used and levels of the voltage output. There is always a trade-off between the number of switches and levels of the output voltage. More number of switches improve the output voltage quality at the cost of the increase in the losses(switching and conduction) and cost while reduced switches count deteriorates output voltage quality. So, it was a rigorous task to choose best-fitted topology which has reduced switches count, the voltage source and improved output voltage quality. A comparison with different MLI topologies is presented in Table-I for selection to integrate the Z-source concept. In Table-I, Num stands for Numbers and NVS is Normalized voltage stress. The first four topologies i.e. FC, NPC, Clamped diode, Alternate NPC has similar normalized voltage source stress but switches, capacitor and diodes voltage stress are different. Moreover, these topologies are either having the diodes and capacitors in the arrangement. The presence of diodes causes the larger voltage drop and reverse recovery losses while in case of more number of capacitors it is quite difficult to balance the voltage [32].

Although Z-source with NPC is integrated in the literature [11], [36] but these topologies are not feasible to integrate the Z-source concept. The topology presented in [35] has no capacitor but it has higher voltage source stress and more number of diodes as compared to the modular multilevel inverter(MMLI). In this topology, 12 switches are used 6 of them have to withstand $0.5V_{in}$ and remaining has to withstand $2V_{in}$. Therefore, among all the topologies, MMLI has following advantages as compared to other topologies presented in Table-I:

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TABLE I: Comparison of Number of Components and Voltage Stress for Selection of Best MLI for Integration of Z-source

	N_{DC}		N_{sw}		N_D		N_C	
	Num	NVS	Num	NVS	Num	NVS	Num	NVS
FC [33]	1*2V_{in}	2	12	12	0	0	6	9
Clamped Double [33]	1*2V_{in}	2	15	15	6	6	6	6
NPC [34]	1*2V_{in}	2	12	12	6	6	6	6
Active NPC [34]	1*2V_{in}	2	18	18	0	0	6	6
[35]	6*V_{in}	6	9	15	3	3	0	0
MMLI for Proposed Integration	2*V_{in}	2	12	15	0	0	0	0

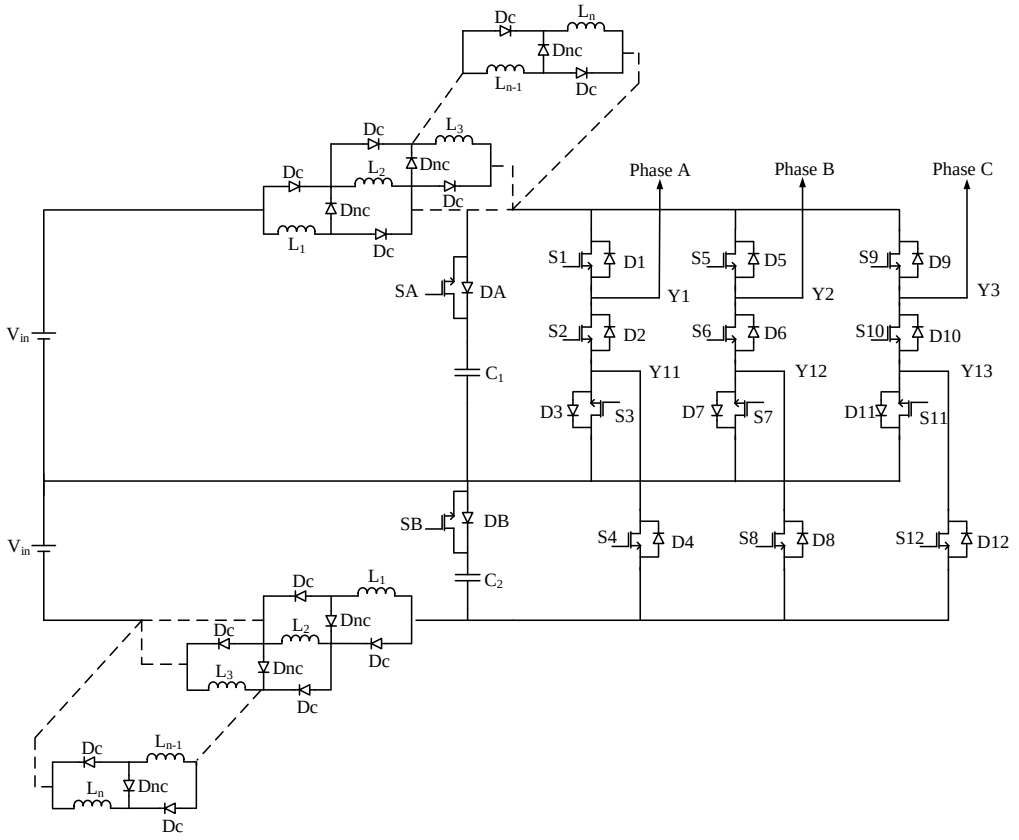

Fig. 2: Proposed Z-source Modular Multilevel Inverter

1) MMLI has lowest total components count.
2) MMLI has lowest total voltage stress.

Therefore, in this paper, to reduce the number of active and passive elements, an MMLI is considered for the integration of Z-source feature.

A generalized switched inductor network is used for integration of Z-source concept. The switched inductor network has reduced number of the passive element as compared to the conventional Z-source network to achieve similar gain. Therefore, it can have better reliability and compactness. In switched inductor network, a snubber circuit is required to mitigate the voltage spikes present due to switching of the inductor between the source and load. For this, a $R-C$ snubber may be used, however, it causes power loss. So, an active snubber circuit is used in the proposed study which consists of an antiparallel switch in series with the capacitor. The active snubber circuit is also exploited to achieve a better gain in DCM. The proposed configuration with generalized switched inductor cell is shown in Fig-2, which is named as switched inductor modular multilevel converter(SL-MMLI). The proposed SL-MMLI has following advantages as compared to Z-source based NPC:

1) SL-MMLI has lower diodes.
2) SL-MMLI has lower capacitive element.

Moreover, the proposed switched inductor multilevel inverter is modular in the sense that it can be extended to as many numbers of levels as required. The proposed topology requires $(n-1)$ modules for achieving n levels with respect to the pole voltage. For example, to achieve three levels with respect to pole, two modules of developed topology are required. Furthermore, the connection diagram for connecting these modules to achieve n-level is shown in Fig-3 assuming that each module has six terminals(Y_1, Y_2, Y_3, Y_{11}, Y_{12}, Y_{13}). However, the larger number of levels may decrease the efficiency of the system.

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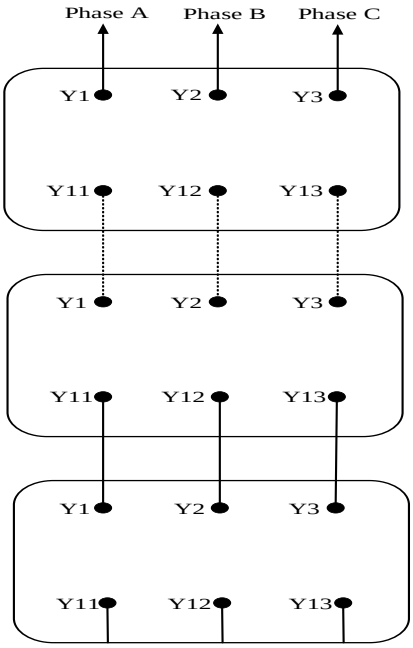

Fig. 3: Extension of the proposed topology for n-levels

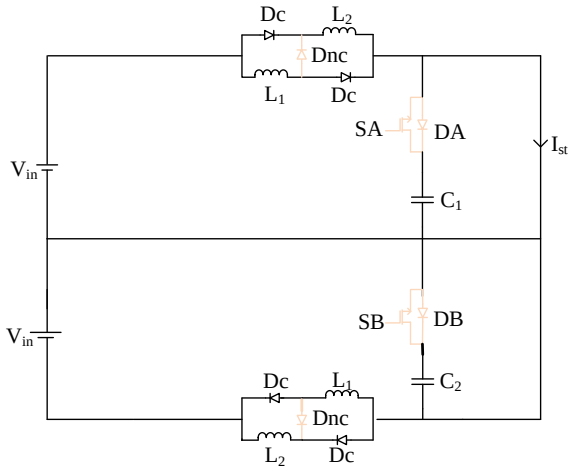

Fig. 4: Full shoot though state

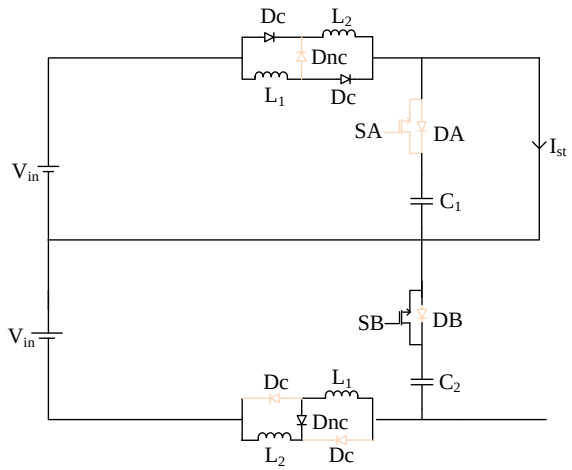

Fig. 5: Upper shoot though state

B. Operation

The operation of the SL-MMLI is divided into two categories: 1) Full shoot through state (FST) 2) Upper shoot through state (UST)/Lower shoot through state (LST)

1) Full shoot through state: In FST, the shoot-through (ST) pulse is applied to all the switches of the same or more leg. Moreover, the antiparallel switches SA and SB are turned off. Consequently, the diodes D_c of both the upper and lower switched inductor network is forward biased and diode D_{nc} of both the upper and lower switched inductor network becomes reverse biased. As a result of this, the inductors L_1 and L_2 in upper half are charged through the switches S_1, S_2 and D_3 and the inductors L_1 and L_2 in lower half are charged through the switch S_4 and D_3 as shown in Fig-4. All the inductors slope is positive during this period. The output voltage produced during this period is zero in all the phases.

2) Upper shoot through state: In UST, ST pulse is only applied to the switches of the upper half in any two legs depending on the switching. The antiparallel switches SA and SB are turned off. Consequently, the diodes D_c of the upper switched inductor network is forward biased and diode D_{nc} of the upper switched inductor network becomes reverse biased. This results in, the inductors L_1 and L_2 in the upper half charged through the switches S_1, S_2 and D_3, as shown in Fig-5 and have positive current slope during this period. The lower half of the inverter operates in the active period during this state. Therefore, the output line voltage produced during this period is zero in any one phase.

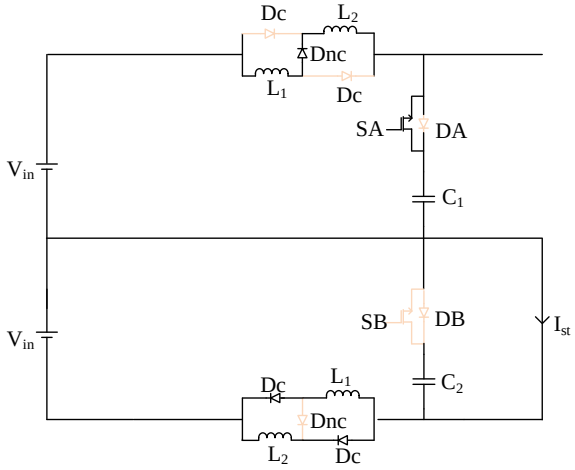

Fig. 6: Lower shoot through state

3) Lower shoot through state: During LST, ST pulse is only applied to the switches of lower half in any two-leg depending on the switching. The antiparallel switches SA and SB are turned off. Due to this, the diodes D_c of the lower switched inductor network is forward biased and diode D_{nc} of the lower switched inductor network becomes reverse biased. Therefore, the inductors L_1 and L_2 in the lower half are charged through the switches S_3 or S_4, as shown in Fig-6 and have positive current slope during this period. The upper half of the inverter operates in the active period during this state. Similar to UST, the output line voltage produced during this period is zero in

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any one phase. The switching pattern for FST and UST/LST is shown in Table-II.

TABLE II: Switching State Under Shoot Through

	UST	LST	FST
Leg 1	S_1, S_2, D_3	S_3,S_4	S_1,S_2,D_3,S_4
Leg 2	S_5, S_6, D_7	S_7,S_8	S_5,S_6,D_7,S_8
Leg 3	S_9, S_{10}, D_{11}	S_{11},S_{12}	S_9,S_{10},D_{11},S_{12}

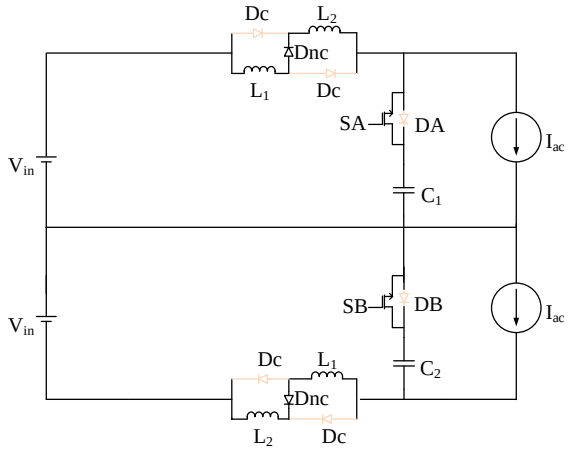

Fig. 7: Active state

4) Active state for CCM: For both the charging period i.e. FST and UST/LST, the active state is similar. ST pulses are removed from the inverter legs during this period and inverter produces a certain output voltage in all the three phases. The switches SA and SB are turned on by non-shoot through pulses. The diode D_{nc} becomes forward biased while diodes D_c are forward biased for both FST and UST/LST. The inductors in the upper half and lower half connected in series and starts freewheeling their respective energy to the load as shown in Fig-7. The slope of the current becomes negative during this period. The switching strategy for the active state is presented in Table-III.

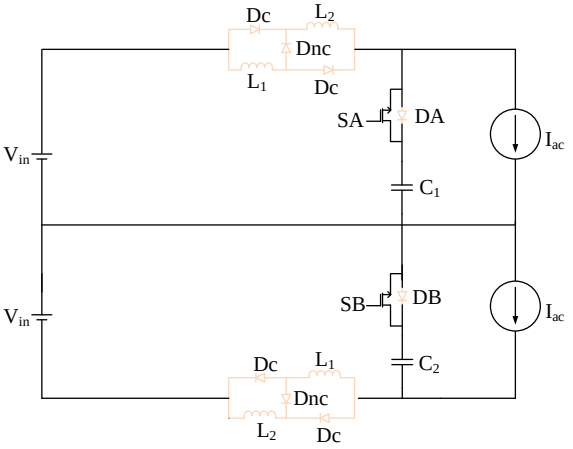

Fig. 8: Active state for DCM

5) Active state for DCM: During this period, the switching of the inverter is similar to the active state described above. The switches SA and SB are still turned on. However, due to the light load condition, the inductor's current becomes equal to zero before the start of the next shoot through period. Therefore, the capacitor C_1 and C_2 serves as a power source to the inverter which maintains the constant voltage across the inverter through the switches SA and SB. As both the diodes D_c are reverse biased so the power never reaches back to the source.

IV. Steady State Analysis of SL-MMLI

For steady-state analysis, all the losses present in the switches and diodes are neglected. Since the average voltage for FST, UST/LST remains the same hence steady-state analysis is performed for UST. So, UST is considered for further analysis. Similarly, it can be applied to the FST and LST. Moreover, all the inductor are considered equal i.e. L_1= L_2=L_3=.....=L_n=L.

A. Boosting Under CCM

The profile for voltage and current for SL-MMLI under CCM is shown in Fig-9i. From Fig-5, during charging, the KVL is written as

$$V_{in} - V_L = 0 \tag{1}$$

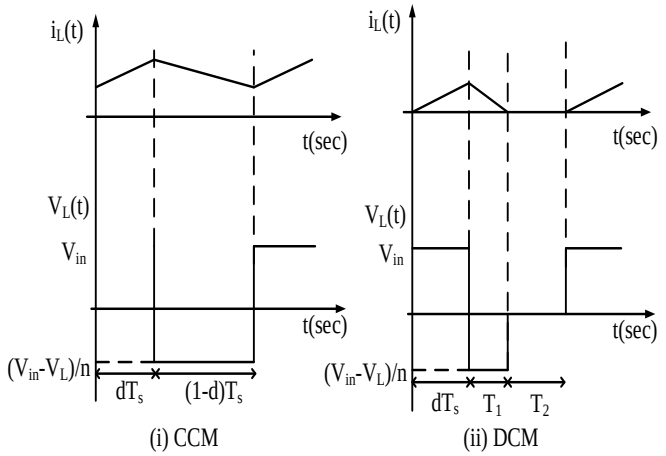

Fig. 9: Steady State waveform for SL-MMLI under CCM and DCM

while in the discharging period, the KVL is

$$V_{in} - nV_L - V_{P1} = 0 \tag{2}$$

By taking the average over a switching period across inductor L, the voltage equation is written as

$$\int_0^{dT_s} V_L dt + \int_{dT_s}^{T_s} V_L dt = 0 \tag{3}$$

By solving the above equation, the output voltage(V_{P1}) is given as

$$V_{P1} = \frac{1 + (n-1)\,d}{1-d} V_{in} \tag{4}$$

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TABLE III: Switching State Under Active State

V_{AB}	V_P	$2V_P$	$2V_P$	$2V_P$	V_P	0	$-V_P$	$-2V_P$	$-2V_P$	$-2V_P$	$-V_P$	0
V_{BA}	$-2V_P$	$-2V_P$	$-V_P$	0	V_P	$2V_P$	$2V_P$	$2V_P$	V_P	0	$-V_P$	$-2V_P$
V_{CA}	V_P	0	$-V_P$	$-2V_P$	$-2V_P$	$-2V_P$	$-V_P$	0	V_P	$2V_P$	$2V_P$	$2V_P$
Switch	S_2,S_3,S_6 S_8,S_9	S_1,S_6 S_8,S_9	S_1,S_6,S_8 S_{10},S_{11}	S_1,S_6 S_8 S_{10},S_{12}	S_1,S_6 S_7 S_{10},S_{12}	S_1,S_5 S_{10},S_{12}	S_2,S_3 S_5 S_{10},S_{12}	S_2,S_4 S_5 S_{10},S_{12}	S_2,S_4 S_5 S_{10},S_{11}	S_2,S_4 S_5,S_9	S_2,S_4 S_6 S_7,S_9	S_2,S_4 S_6 S_8,S_9

where V_{P1} is DC link voltage and n is switched inductors. The average value of V_{P1} = V_{P2}, so they can be written as V_P. Therefore, as per the switching strategy of SL-MMLI, the available voltage at the output terminal will be equal to either V_P or $2V_P$ instead of V_{in} or $2V_{in}$. This means that the boosted voltage will be available at the output. For different switched inductor cell, the gain of the SL-MMLI is plotted in Fig-10.

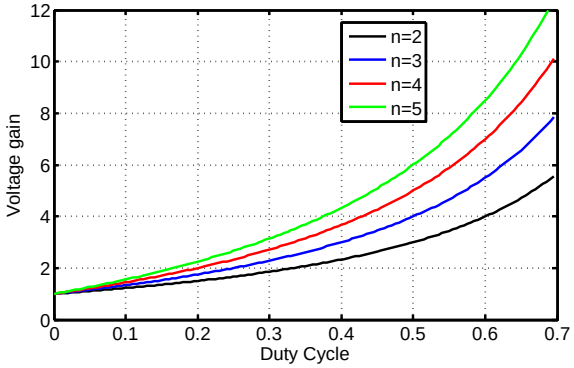

Fig. 10: Gain of SL-MMLI at different cell

B. Boosting Under DCM

For the DCM period, the KVL equations for charging and discharging period will be the same as CCM. However, when the SL-MMLI switches into DCM, the voltage across the inductors becomes equal to zero. The profile for voltage and current for the DCM period is shown in Fig-9(ii). The voltage across the inductor in DCM is written as

$$V_L = 0 \tag{5}$$

By taking the average over a switching period, the voltage equation is

$$\begin{aligned} &\int_0^{dT_s} V_{L1}dt + \int_{dT_s}^{T_1+dT_s} V_{L2}dt + \int_{T_1+dT_s}^{T_s} V_{L3}dt = 0 \\ &ndT_sV_{in} + (1-d-d_2)\,T_s\,(V_{in} - V_{P1}) = 0 \end{aligned} \tag{6}$$

By solving Equ-(1), (2) and (6), the output voltage is given as

$$V_{P1} = \frac{1+(n-1)\,d-d_2}{1-d-d_2}V_{in} \tag{7}$$

where d_2 is the duty cycle which represents the DCM period. Equ-(7) indicates that as SL-MMLI goes deeper into DCM, the gain kept on increasing. A comparative analysis is presented in Fig-11 for CCM and DCM. Theoretically, it is clear that the DCM gain is higher than CCM for similar number of inductor cells (n)(for e.g. at d=0.5 and d_2=0.3, CCM gain =3 while DCM gain=6).

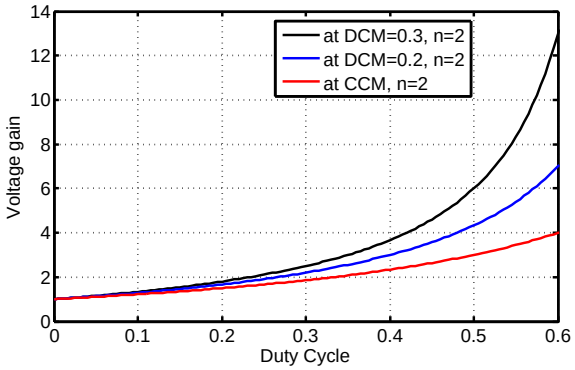

Fig. 11: Comparison of gain for SL-MMLI under CCM and DCM

V. Control of Proposed Converter

There are mainly two modulation techniques that can be applied to control the MLI. These are classified as low-frequency modulation(LFM) and high-frequency modulation(HFM). The selection of these techniques depends on the requirements. Lower switching loss can be ensured in case of LFM while HFM provides better quality output. However, for Z-source based MLI, the HFM techniques are useful as it helps in reducing the size of the passive elements. Therefore, the HFM technique is chosen for further analysis. There are different HFM techniques such as sinusoidal pulse width modulation (SPWM), space vector pulse modulation and optimal pulse width modulation. In this paper, the SPWM technique has opted for pulse generation. The control pulse generation can be achieved by comparing a triangular carrier wave with sinusoidal signals.

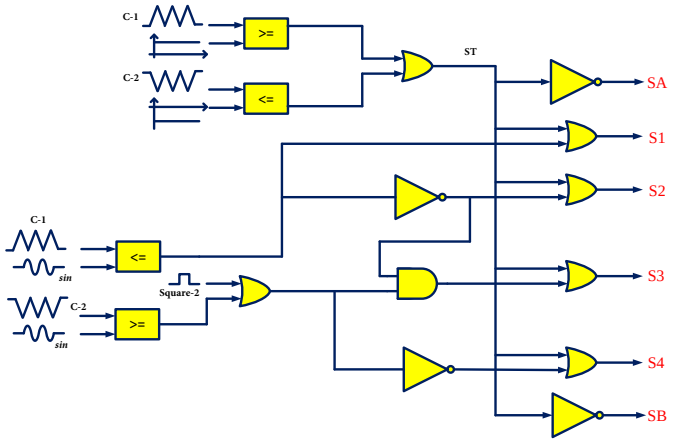

Fig. 12: Pulse generation for SL-MMLI under FST

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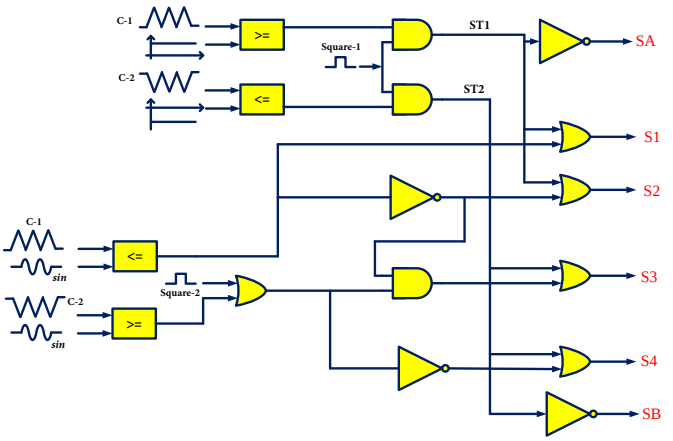

Fig. 13: Pulse generation for SL-MMLI under UST and LST

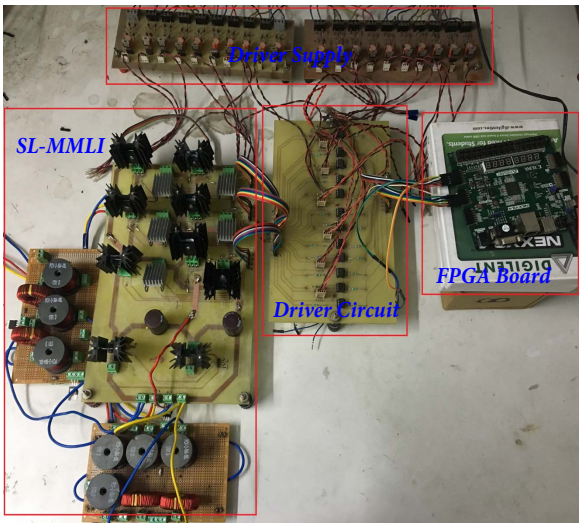

Fig. 14: Experimental set up for SL-MMLI

However, this technique has a higher THD. Since, phase deposition(PD) technique is suitable for reducing the THD [37], [38], therefore, PD technique is considered for pulse generation. In PD, two carrier waves which are in phase and operating at the same frequency but distinct in amplitude are compared with the sinusoidal signal. The pulse generation is done to achieve two distinct shoot through techniques i.e. FST and UST/LST. The pulse generation for phase A is presented in Fig-12. For phase B and phase C, pulses are generated by shifting the sinusoidal signal by 120° and 240°, respectively along with mixing ST pulse in all the switches.

For phase A, the UST pulse generation is shown in Fig-13. However, for phases B and C, two steps must be followed: 1) The ST1 and ST2 generation by shifting the square wave by 120° and 240° for B and C, respectively. 2) Generation of pulses by shifting the sinusoidal signal by 120° and 240° for B and C, respectively. Then the two pulses generated for B and C are mixed by the procedure described for phase A in Fig-13 to produce a resultant pulse for switches.

VI. Experimental Results

For validation of the proposed idea, an experimental prototype is designed and developed. The prototype for SL-MMLI is designed and the printed hardware is shown in Fig-14.

TABLE IV: Converter Parameters in CCM

Each Inductor	1.12 mH
Each Capacitor	100 μF
Switching frequency	20 kHz
Output frequency	50 Hz
Resistive load	30 Ω
Inductive load	40 Ω, 50 mH
Input voltage	80 V/source
Output voltage	125 Vrms
Maximum Power	520 Watt

For the implementation of control logic, the FPGA board is used in hardware. The semiconductor devices used in the experimental setup are listed in Table-V. The experimental results show the glitches. The sources of generating these glitches are switching of inductor and presence of parasitic present due to connecting wires. These glitches are appearing in the output profile because there is no filter connected at the output. These glitches are also observed in the previous work [11]. These glitches will be removed by placing a filter. The performance of SL-MMLI is tested under two different operating modes which is explained as follows:

TABLE V: Components Used

Component	Manufacturer	Model No.	Rating
MOSFET	Semiconductor	STP33N60DM2	600V, A
Diode	Semiconductor	STPS60SM200CW	200V, 30A
Capacitor	Multicomp	MCKSK400M101K32S	400V, 100μF
Inductor	Coilcraft	PCV-2-564-082	7A, 1.12μH

A. Performance Under CCM

For CCM validation, following parameters are selected: L_1=L_2=1.12mH, C_1=C_2=100μF and V_{in}=80 V/each, d=0.2, m=0.8, f_s=20kHz, f_o=50Hz, resistive load-R=30Ω, inductive load-R=40Ω, L=50mH. At first, the SL-MMLI is tested for FST condition. The experimental results are shown in Fig-15. The line to line voltage for FST is shown in Fig-15a which has five levels (-V_P, -2V_P, 0, V_P and 2V_P). The maximum line to line voltage is 235 V according to Equ-(4). The rms value obtained during this period is 116 V. The profile of inductors current is shown in Fig-15b. All the inductors are charged and discharged simultaneously which proves the FST condition. Fig-15c and Fig-15d show the profile of phase voltage and phase current under resistive loading. The voltage and current in all three phases are in phase, however, due to some inductive effect of leads, the profile of inductor current is not exactly similar to phase voltage. Fig-15e represents the profile of inductor current for inductive loading. Fig-15f and Fig-15g show the phase voltage and current in case of an inductive load. The phase difference between the voltage and current indicates the presence of the inductive load. In Fig-15h, the experimental THD profile of line to line voltage is presented which is 75% without using the filter at output [39].

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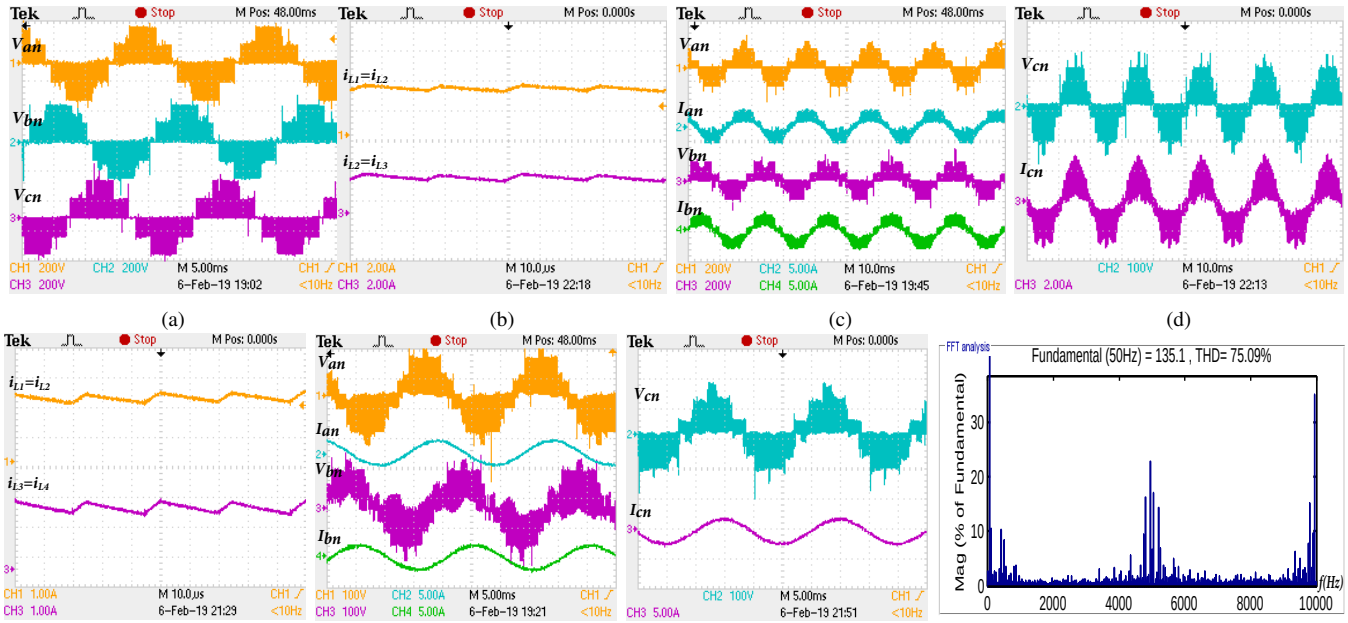

Fig. 15: CCM: Operation under FST a) Line to Line voltage b) Inductors current-resistive load c) Phase voltage and current for phases 'a' and 'b'-resistive load d) Phase voltage and current for phase 'c'-resistive load e) Inductors current-inductive load f) Phase voltage and current for phases 'a' and 'b'-inductive load g) Phase voltage and current for phase 'c'-inductive load h) FFT analysis

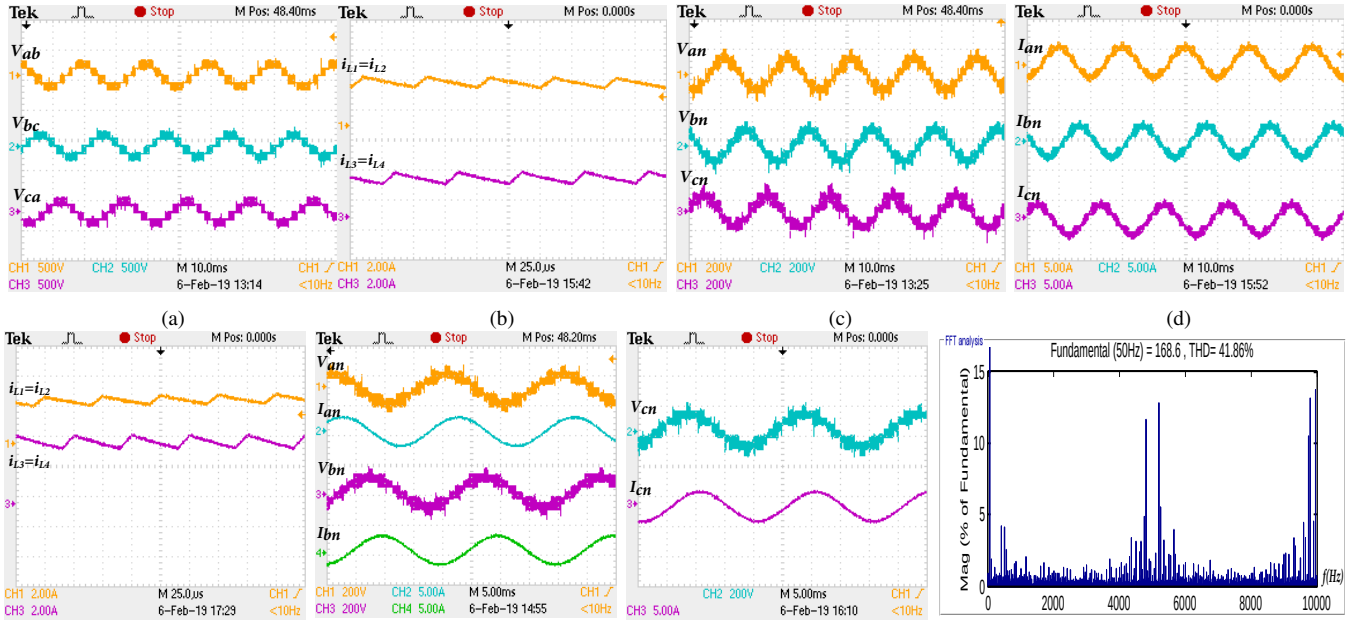

Fig. 16: CCM: Operation under UST/LST a) Line to Line voltage b) Inductors current-resistive load c) Phase voltage for phases 'a', 'b' and 'c'-resistive load d) Phase current for phases 'a', 'b' and 'c'-resistive load e) Inductors current-inductive load f) Phase voltage and current for phases 'a' and 'b'-inductive load g) Phase voltage and current for phase 'c'-inductive load h) FFT analysis

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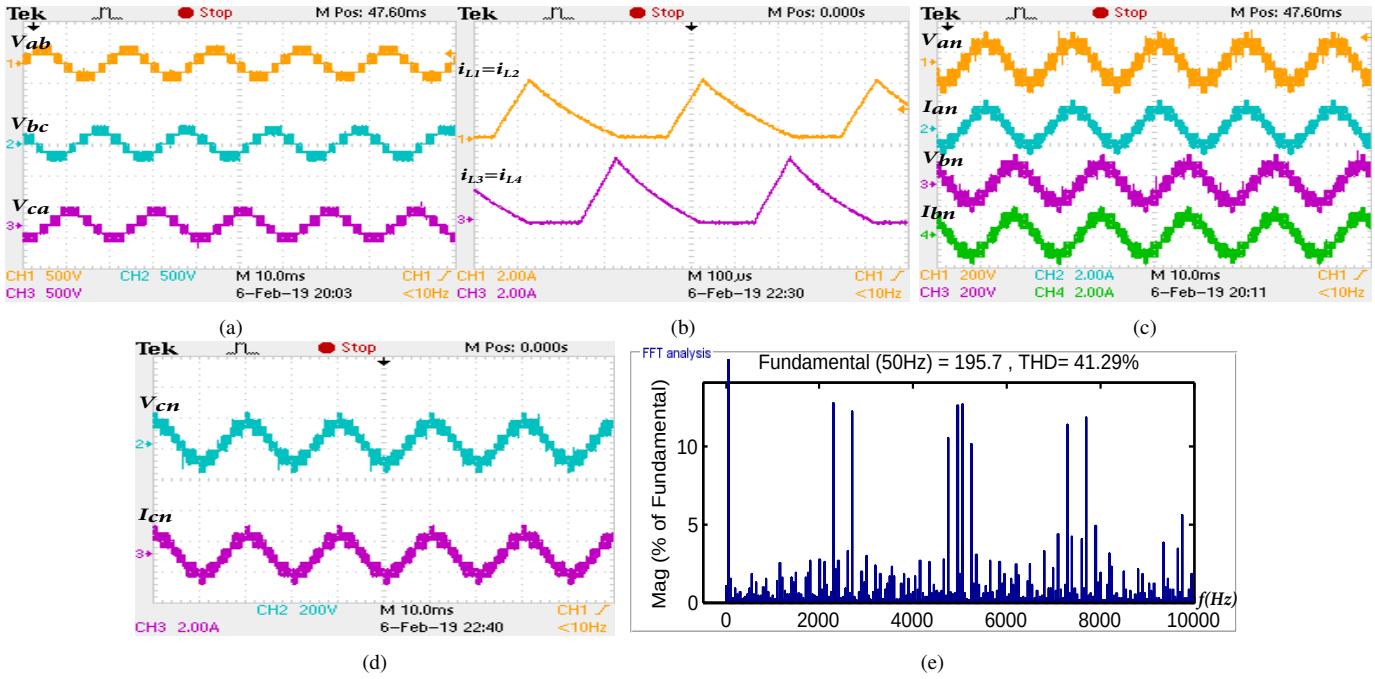

Fig. 17: DCM: Operation under UST/LST a) Line to line voltage b) Inductors current c) Phase voltage and current for phases 'a' and 'b' d) Phase voltage and current for phases 'c' e) FFT analysis

To achieve better THD, SL-MMLI is operated for UST/LST condition. The experimental results pertaining to this state are shown in Fig-16. Fig-16a shows the line to line voltage which has a maximum magnitude of 235 V. However, the rms value obtained in this period is equal to 125 V which is higher than FST due to the reduction in the period for zero voltage. The inductor currents for the resistive load is shown in Fig-16b. It is observed that the instant of charging and discharging period both the inductor is different. Therefore, at a time only one half of the inverter is subjected to shoot through state. The phases voltage and current for the resistive load is shown in Fig-16c and Fig-16d. The voltage and current are in the same phase, however, phases current may have a different shape than the voltage owing to the presence of small inductance. Further, SL-MMLI is operated for the inductive load. The inductor current and phases voltage, the current is shown in Fig-16e and Fig-16f, Fig-16g respectively. The load current is lagging by 25° from the respective voltage. Further, to show the effectiveness of UST/LST, experimental THD is shown in Fig-16h. The THD in case of UST/LST is reduced by 34% which is a huge improvement over FST and therefore, requires smaller filter to produce smooth voltage profile.

TABLE VI: Converter Parameters in DCM

Each Inductor	1.12 mH
Each Capacitor	100 μF
Switching frequency	5 kHz
Output frequency	50 Hz
Resistive load	200 Ω
Input voltage	80 V/source
Output voltage	154 Vrms
Output Power	120 Watt

B. Performance Under DCM

The SL-MMLI is operated in DCM to achieve higher voltage gain. Normally, DCM occurs under light loading condition or designed accordingly which are commonly resistive in nature. Therefore, for validation of DCM, the SL-MMLI is only operated under light resistive loading condition. The parameters for DCM are same except: f_s=5kHz and $R_{perphase}$=200 Ω. Moreover, DCM is only validated for UST/LST as FST creates higher THD and is not suitable for application purpose. The experimental results corresponding to DCM are shown in Fig-17. The line to line voltage during DCM is shown in Fig-17a which has a higher magnitude by 45 V as compared to CCM (according to Equ-(7)). During this period, the inductors, current reaches to zero and stays at zero for the finite duration before the start of next ST as shown in Fig-17b. The phase voltage and phase current for the DCM period are shown in Fig-17c and Fig-17d, respectively. These voltage and currents are in the same phase. Furthermore, the THD analysis in the DCM period (for UST/LST) is presented in Fig-17e. The THD produced during this period is similar to CCM (for UST/LST) i.e. 41.26%.

VII. Performance in terms of Efficiency

In the literature, cascaded and conventional (i.e. NPC or ANC) three-phase Z source multilevel inverters are reported, however, cascaded MLI is different from the configuration proposed in this paper and also having many components. Therefore, it is not suitable to compare the proposed converter with them. Only Z-source NPC or ANPC, which are closed to the proposed converter, are considered for the comparison in this paper. It is assumed that all the converters i.e. NPC, ANPC and proposed converter has similar Z-source network

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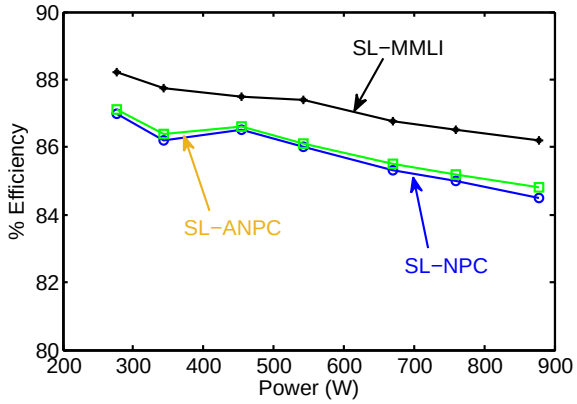

Fig. 18: Comparison in Continuous Current Mode

(i.e. switched inductor cell) at the boosting stage. The parasitic considered for the efficiency calculation is: internal resistance for each inductor is 0.225 Ω, internal resistance for capacitance is 0.12 Ω, switches internal resistance is 0.13 Ω, switches diode voltage drop is 0.7 V, diodes forward resistance is 1.8 V and diodes internal resistance is 0.1 Ω. The efficiency is compared in both CCM and DCM mode for all three converters. Due to the lesser number of components in the proposed SL-MMLI, the efficiency for the SL-MMLI is higher than SL-NPC and SL-ANPC in both CCM and DCM. Therefore, the proposed converter has better prospect as compared to SL-NPC and SL-ANPC.

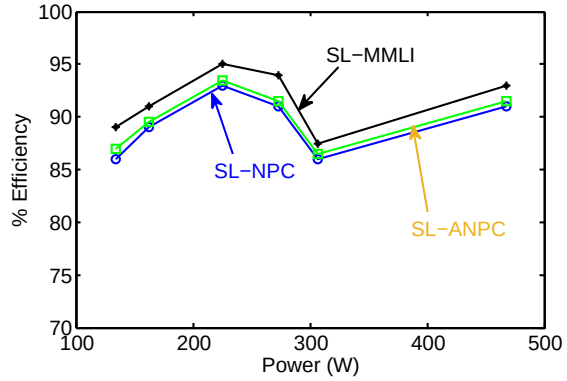

Fig. 19: Comparison in Disontinuous Current Mode

VIII. Conclusion

A modular multilevel inverter is proposed which utilizes the Z-source concept. The switched inductor network is used as a boosting network in the generalized sense which helps in providing adequate voltage gain. To control SL-MMLI, two control techniques, i.e. FST and UST/LST, are proposed. The converter is validated in hardware for both the control techniques, operating modes and under different loading conditions. Based on the experimental and analytical study, the following conclusions are drawn:

1) In both the states, the SL-MMLI operates satisfactorily for both resistive and inductive load.
2) FST produces 75% THD in line to line voltage.
3) UST/LST generates only 41% THD in line to line voltage.
4) In DCM, higher voltage gain is achieved.
5) Due to Z-source integration, SL-MMLI produces 235 V in CCM as compared to 160 V in MMLI.
6) In DCM, SL-MMLI produces 280 V as compared to 160 V in MMLI.
7) The SL-MMLI has the lower component count, lower normalized voltage stress than the NPC and ANPC,
8) The SL-MMLI has better efficiency than the NPC and ANPC.

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